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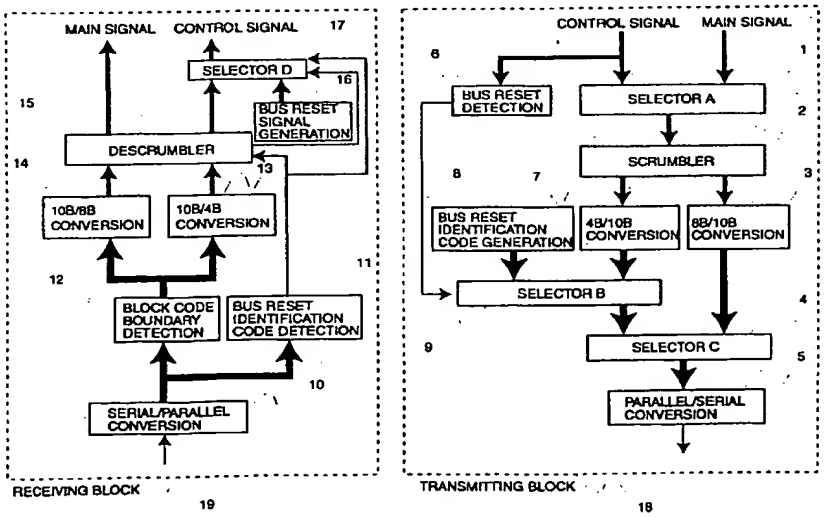
(54) Encoding circuit and method of detecting block code boundary and establishing synchronization between scrambler and descrambler

(57) The present invention comprises the bus reset detection circuit (6) detecting a bus reset signal from the network initiation/control state machine, the bus reset identification code generation circuit (8) and the bus reset identification code detection circuit (11) detecting a bus reset identification code and the bus reset signal generation circuit (16) which outputs a bus reset signal to the network initiation/control state machine.

FIG.1



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Description

[0001] The present invention relates to an encoding circuit used in a serial bus (for example, a serial bus standardized by the Institute of Electrical and Electronics Engineers [IEEE] Standard for a High Performance Serial Bus - the IEEE Std 1394 - 1995 -, hereafter called a 1394) connectable to a personal computer (hereafter, a PC) and electronic devices.

[0002] A network using a 1394 for the purpose of transmitting a control signal and a main signal between a PC and peripheral devices such as a printer, a hard disk, a scanner and the like, or between a PC and an AV (Audio Visual) electronic device (hereafter, call a 1394-equipped terminal device a node) is supposed.

[0003] A node has a port (hereafter, called a DS port) using an encoding method of transmitting a data signal and a strobe signal at the same time, which is called a DS-Link encoding method (making reference to the IEEE Std. 1394-1995 pp.34). The DS-Link encoding method has a characteristic that a clock can be regenerated by generating an exclusive OR of two (2) signals on the receiving side on the one hand, but it has also a defect, on the other hand, that a transmitting signal transmitted from a transmitting node can not be regenerated precisely on the receiving side in the case where a phase difference between two signals is generated on the receiving side due to a difference between propagating speeds of the two signals because two signals are transmitted at the same time and in the case where a distance between nodes becomes long. Therefore, a distance between nodes is limited within several meters in the case where a DS-Link encoding method is used.

[0004] On the other hand, in the case where a distance between nodes extends over for scores of meters, a node has a port (hereafter, called a serial port) having an encoding circuit for the purpose of performing a serial transmission. However, in this case, it is necessary to regenerate a clock out of a transmission signal using a clock recovery circuit on the receiving side.

[0005] In Fig.6, a constitution of nodes having DS ports and serial ports are shown. The port(a)s, (b)s are DS ports, and the port(c)s is serial ports. The present invention relates to a serial port, description about a DS port is omitted (making reference to the IEEE 1394-1995 pp.76 in detail). As for the node A and the node B, serial ports are connected each other by way of a transmission path. Each bode has the network initiation/control state machine 21 performing the acquisition of the transmission right to the network at the time of the initiation of the network and during the usual operation. A serial port is composed of the transmitting block 18, the receiving block 19 and the port initiation block 20.

[0006] The transmitting block 18 transmits a control signal outputted from the port initiation block 20 until the initiation of the port is completed. After the completion of the initiation of the port, the transmitting block 18 transmits a control signal outputted from the network initiation/control state machine.

[0007] The receiving block 19 passes a received control signal to the port initiation block 20 until the initiation of the port is completed. The receiving block 19 passes a control signal to the network initiation/control state machine after the completion of the initiation of the port.

[0008] The port initiation block 20 acknowledges that ports were connected each other using a Port_Status signal at the time when the initiation of the ports was completed and a communication connecting the ports each other could be available to the upper network initiation/control state machine 21. The network initiation/control state machine 21 which has detected a change of a Port_Status signal starts the initiation of the network by transmitting a bus reset signal. The present invention relates to a serial port, description about the initiation of the network is omitted (making reference to the IEEE 1394-1995 pp.98-112 in detail).

[0009] The operation procedure of the port initiation block 20 is shown in Fig.7. The transmitting block operates at S100 (baud rate 125Mb/s) of the lowest transmitting speed at the initiation of the ports. Until an output clock of a PLL (Phase Locked Loop) circuit generating a transmitting clock is stabilized (locked) at 125MHz after the power of the nodes is switched on, since the transmitting block remains in a state of resetting, there is no output from the port. Once an output of the transmitting PLL is stabilized, the port initiation block 20 outputs a Request/Grant code (0001) in series as a control signal. A list of control signal codes is shown in Fig.8. A opposed node also operates in the similar procedure, receives a Request/Grant code from the other opposed node. Upon receiving a Request/Grant code, in the receiving block, a clock recovery circuit generating a receiving clock out of a received signal starts to retract a signal, and waits for being capable of stably generating (locking) a receiving clock. After a clock recovery circuit is locked, detecting a boundary of a block code out of a signal serial-transmitted is performed. After the detection of a boundary of a block code, the synchronization between a scrambler which is located in the receiving block of the opposed node and a descrambler (for example, in Fig.6, the scrambler of the node A and the descrambler of the node B, or the scrambler of the node B and the descrambler of the node A) is obtained. After the establishment of the synchronization between a scrambler and a descrambler, an IDLE code (0000) is outputted as a control signal from the port initiation block. The node which has detected an IDLE code recognizes that a clock recovery circuit of the opposed node being locked, the detection of a block code boundary and the establishment of the synchronization between a scrambler and a descrambler are completed.

[0010] Next, in order to arbitrate a transmitting speed between ports, the port initiation block 20 outputs a SPEED

code indicating the maximum transmitting speed that its port can transmit as a control signal. After receiving a SPEED code from the opposed node, the port initiation block 20 compares the SPEED code from the opposed node with the SPEED code transmitted by itself, and sets a transmitting speed of the ports at the lower transmitting speed. At that time, in the case where the transmitting speed is set at S100 (a plurality of transmitting speeds are standardized by the IEEE 1394, the lowest transmitting speed is defined as S100:100Mb/s. Besides this, S200: 200Mb/s, S400:400Mb/s and the others are standardized.), a Port_Status signal is set in order to acknowledge the completion of the initiation of the port to the upper network initiation/control state machine. In the case where the transmitting speed is not set at S100, a speed arbitration flag indicating the completion of the arbitration of a transmitting speed is set, and after a transmitting PLL circuit and a clock recovery circuit are reset, the procedure of the initiation of the port is performed again. After the completion of the steps up to the establishment of the synchronization between a scrambler and a descrambler, a Port_Status signal is set, then, the initiation of the port is completed.

[0011] For example, if the maximum transmitting ability of the node A is S100 and the maximum transmitting ability of the node B is S200, the node A transmits a code indicating that the maximum speed of the node A is S100, the node B transmits a code indicating that the maximum speed of the node B is S200. In the node B, as a SPEED code received from the node A is recognized, a transmitting speed of the serial port of the node B is set at S100. Since both the node A and the node B already operates at S100, the operations of the node A and the node B subsequently transfer to the usual operations. On the other hand, in the case where the maximum transmitting speed is set at S200 in both the node A and the node B, a transmitting speed of the serial port of both the node A and the node B is set at S200. After that, in order to make the PLL circuit and the clock recovery circuit operate at S200, the procedure of the initiation is performed again at S200, and after the completion of the operations up to a step of the establishment of the synchronization between a scrambler and a descrambler, the operations of the node A and the node B transfer to the usual operations.

[0012] Next, the operation of the transmitting block and the receiving block at the time of the initiation of the port will be described below. Constitutions of the transmitting block 18 and the receiving block 19 are shown in Fig.9. In the transmitting block 18, a control signal and a main signal is switched by the selector A1, and codes are randomized by the scrambler 2. As for randomized codes, a control signal is converted into a block code of 10 bits by the 4B/10B conversion circuit 3, and a main signal is converted into a block code of 10 bits by the 8B/10B conversion circuit 3. It should be noted that a list of conversion of the 4B/10B conversion circuit 7 is shown in Fig.10 (as for 8B/10B conversion table, making reference to P1394b Draft0.05 pp.68-70). A control signal and a main signal which are switched by the selector C are passed to the parallel/serial conversion circuit. After a block code is converted into a serial signal by the parallel/serial conversion circuit 5, and the serial signal is transmitted. In the receiving block 19, a received serial signal is converted into a parallel signal by the serial/parallel conversion circuit 10, the detection of a block code is performed by detecting the coincidence of a pattern of 10 bits with a symbol C4 (=0010001111) or a symbol C11 (=1101110000) using the block code boundary detection circuit 12. After that, a main signal is converted by the 10B/8B conversion circuit, and a control signal is converted by the 10B/4B conversion circuit, the original control signal or the original main signal are restored by the descrambler.

[0013] The block code boundary detection circuit performs the detection of a block code boundary by detecting the coincidence with a C4 and a C11 at the time of the initiation of the port. Since the same pattern with those of a C4 and a C11 exists in a main signal, the detection of a boundary is not performed not so as to perform an erroneous detection during the usual operation.

[0014] A scrambler is constituted using a generating polynomial $G(x) = X^{11} + X^9 + 1$ as shown in Fig.11, and a pseudo-randomized signal is outputted as a coefficient of X^7. Control signals (S R Q P) and main signals (H G F E D C B A) are randomized by their assuming exclusive ORs with coefficients of a scrambler register as shown in Fig.12. At this time, the value of the scrambler register S(10:0) is calculated by an equation of $S_{k+1}(10:0) = T \cdot S_k(10:0)$. Here, k expresses a clock, the value of register $S_{k+1}(10:0)$ is calculated by the product of the foregoing value $S_k(10:0)$ and T. T is expressed by the following expression.

[EXPRESSION 1]

		0	0	0	0	0	0	0	0	1	0	0	
		0	0	0	0	0	0	0	0	0	1	0	
		0	0	0	0	0	0	0	0	0	0	1	
		1	0	1	0	0	0	0	0	0	0	0	

(continued)

[EXPRESSION 1]

$$T = \begin{bmatrix} 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 \end{bmatrix}$$

[0015] The establishing procedure of the synchronization between the scrambler register 23 and the descrambler register 24 will be described below with reference to Fig.13. The scrambler and the descrambler use the same signals as for a control signal and a main signal, the operation of establishing the synchronization between the scrambler and the descrambler is performed at the time of transmitting a control signal. In the case of being for synchronization between the scrambler and the descrambler, a train bit for adjusting the value of the descrambler register is set in the descrambler 15. In this case, the value of the descrambler register D(10:0) is expressed by the expression of $D_{k+1}(10:0) = T \cdot D_k(10:0) + C$. Here, C is expressed using a descrambler output S", Q" and a train bit by the expression of C = [0,0,0,0,S" and train,0,S" and train,0,Q" and train,0,Q" and train]^t. At the time of the initiation of the port, at first, a Request/Grant(S R Q P) = (0001) is inputted as a control signal, a train bit is set. Of this case, the variations of the values of a scrambler and a descrambler and descrambler outputs are shown in Fig.14. At the time of CKL=0, for example, since the value of scrambler register is (10000000000) and the value of descrambler is (01001011111), suppose that the synchronization between the scrambler and the descrambler is not established. Therefore, the descrambler output (S" R" Q" P") is (0010), and this code is different from the inputted control signal (0001). Since a train bit is set and adjustments for descrambler register are added, the value of the descrambler are adjusted as CLK proceeds. At the time of CLK=5, the synchronization between a scrambler and a descrambler is established, both of register values is (10101001000), a descrambler output which is the same with an inputted code (0001) is obtained. Hereafter, as far as the same control signal being inputted, even in a state of a train bit being set, the synchronization is not lost. But in the case where the control signal is changed, the synchronization is lost, therefore, before the control signal is changed, a train bit is reset. Consequently, at the time of the completion of the initiation of port, a train bit was previously reset.

[0016] However, even after the completion of the initiation of the port, since an error of a block boundary and loss of the synchronization between the scrambler and the descrambler due to the noises and the like may be generated, it is necessary to perform the detection of a block code boundary, setting of a train bit and the re-establishment of the synchronization between a scrumble and a descrambler even after the completion of the initiation of the port. In the prior art, codes are randomized on the transmitting side, in the case where an error of a block boundary and loss of the synchronization between a scrambler and a descrambler are generated, since a code of the transmitting side can not be recognized on the receiving side, an error of a block boundary and loss of the synchronization can not be detected. Therefore, a timing of performing the re-detection of a block boundary and the re-establishment of the synchronization between a scrambler and a descrambler after the completion of the initiation of the port is ambiguous.

[0017] Moreover, in the case where an error of a block boundary and loss of the synchronization between a scrambler and a descrambler are generated, even if they can be detected, performing the procedure of the initiation of the port again means that changes (set/reset and reset/set) of a Port_Status signal are generated two times until the usual operation is restored. Specifically, it is not efficient since the initiation of the network and the arbitration of the transmitting speed must be performed two times.

[0018] It is an objective of the present invention to solve the problems described above.

[0019] Moreover, the objective of the present invention is to provide a technology of an encoding circuit for the purpose of performing the re-detection of a block code boundary and the re-establishment of the synchronization between a scrambler and a descrambler without performing the procedure of initiation of the port in the case where an error of a block code boundary and loss of the synchronization between a scrambler and a descrambler are generated due to the noises and the like during the usual operation.

[0020] An encoding circuit of the present invention for achieving the objective described above is characterized in that it comprises a bus reset detection circuit (reference numeral 6 of Fig.1) detecting a control signal outputted from the network initiation/control state machine is a bus reset signal which performs the initiation of the network, a bus reset identification code generation circuit (reference numeral 8 of Fig.1) generating a bus reset identification code for replacing

a code of a first several clocks interval of a continuous bus reset signal, and still more for detecting a bus reset and a block code boundary on the receiving side, a bus reset identification code detection circuit (reference numeral 11 of Fig.1) detecting a bus reset identification code and setting a train bit of a descrambler and a bus reset signal generation circuit (reference numeral 16 of Fig.1) outputting a pseudo bus reset signal to the network initiation/control state machine during the re-establishment of the synchronization of a descrambler.

[0021] An encoding circuit of the present invention is characterized in that it comprises a bus reset detection circuit (reference numeral 6 of Fig.5) detecting a control signal outputted from the network initiation/control state machine is a bus reset signal which performs the initiation of the network and generating a trigger signal which performs re-detection of block code boundary, a block code boundary detection circuit (reference numeral 12 of Fig.5) setting a train bit after the re-detection of block code boundary and a bus reset signal generation circuit (reference numeral 16 of Fig.5) outputting a pseudo bus reset signal to the network initation/control state machine during the re-establishment of the synchronization of the descrambler.

[0022] According to the present invention as described above, the re-detection of a block code boundary and the re-establishment of the synchronization between a scrambler and a descrambler can be performed, and by an acknowledgment that a bus reset is outputted from the transmitting side using a signal which is not randomized to the receiving side, the initiation of the network and the initiation of the serial port can be performed at the same time using a bus reset signal performing the initiation of the network.

[0023] This and other objectives, features and advantages of the present invention will become more apparent upon a reading of the following detailed description and drawings, in which:

Fig. 1 is a block diagram showing an encoding circuit of the first embodiment of the present invention;
Fig. 2 is a block diagram showing operations of nodes having encoding circuits of the present invention;
Fig. 3 is a diagram showing examples of outputs of each functional block of the transmitting block;
Fig. 4 is a diagram showing examples of outputs of each functional block of the receiving block;
Fig. 5 is a block diagram showing an encoding circuit of the second embodiment of the present invention;
Fig. 6 is a diagram showing a basic constitution and its connecting configuration of nodes;
Fig. 7 is a flowchart showing the procedure of the initiation of the serial port;
Fig. 8 is a list showing control signal codes and their significance;
Fig. 9 is a block diagram showing a conventional transmitting/receiving section of a serial port;
Fig. 10 is a list of conversion describing an operation of 4B/10B conversion;
Fig. 11 is a diagram showing a constitution of a shift register which is used in the scrambler and the descrambler;
Fig. 12 is a diagram showing the relationship (operation of scrambler) between a scrambler register and a main code or between a scrambler and a control code;
Fig. 13 is a diagram showing the relation between a scrambler and a descrambler; and Fig. 14 is a list describing an example of an operation of a descrambler.

[0024] Next, the embodiments of the present invention will be described with reference to the drawings.

[0025] Fig.1 is a block diagram showing an encoding circuit of the first embodiment of the present invention.

[0026] In Fig.1, an encoding circuit is broadly divided into two (2) sections, the transmitting block 18 and the receiving block 19. The transmitting block 18 is composed of the selector A1, the scrambler 2, the 8B/10B conversion circuit 3, the 4B/10B conversion circuit 7, the selector C4, the parallel/serial conversion circuit 5, the bus reset detection circuit 6, the bus reset identification code generation circuit 8 and the selector B9. On the other hand, the receiving block 19 is composed of the serial/parallel conversion circuit 10, the block code boundary detection circuit 12, the 10B/8B conversion circuit 14, the 10B/4B conversion circuit 13, the descrambler 15, the bus reset identification code detection circuit 11, the bus reset signal generation circuit 16 and the selector D17.

[0027] The selector A1 has a function of switching back and forth between a control signal and a main signal for the purpose of using a common scrambler by a control signal and a main signal.

[0028] The scrambler 2 has a function of randomizing a data sequence of control signals or main signals.

[0029] The 8B/10B conversion circuit 3 has a function of converting a main signal of 8 bits into a code of 10 bits.

[0030] The 4B/10B conversion circuit 7 has a function of converting a control signal of 4 bits into a code of 10 bits.

[0031] The bus reset detection circuit 6 has functions of detecting a bus rest signal in a control signal and outputting a signal for the purpose of switching the selector B9.

[0032] The bus reset identification code generation circuit 8 has a function of generating a special code which is not used in a control signal and a main signal used for the purpose of detecting a bus reset signal on the receiving side.

[0033] The selector B9 has functions of usually outputting a signal from the 4B/10B conversion circuit 7 and outputting a signal from the bus reset identification code generation circuit 8 for several clocks interval after a bus reset signal is detected by the bus reset detection circuit 6.

[0034] The selector C4 has a function of switching back and forth between a main signal and a control signal.

[0035] The parallel/serial conversion circuit 5 has a function of converting a parallel signal of 10 bits into a serial signal.

[0036] The serial/parallel conversion circuit 10 has a function of converting a serial signal from the transmission path into a parallel signal.

[0037] The block code boundary detection circuit 12 has functions of detecting a boundary of a block code (for example, a code of 10 bits) and outputting a parallel signal in a block unit from a boundary to another boundary after the detection of a boundary.

[0038] The 10B/8B conversion circuit 14 has a function of converting a block code of 10 bits which is a main signal into a code of 8 bits.

[0039] The 10B/4B conversion circuit 13 has a function of converting a block code of 10 bits which is a control signal into a code of 4 bits.

[0040] The bus reset identification code detection circuit 11 has functions of detecting a bus reset identification code, setting a train bit, and furthermore, outputting a signal for the purpose of switching the selector D.

[0041] The descrambler 15 has a function of converting a code randomized on the transmitting side into the original code which is not randomized.

[0042] The bus reset signal generation circuit 16 has a function of generating a bus reset signal (0101) as a control signal.

[0043] The selector D has a function of switching back and forth between an output of a descrambler and an output of the bus reset signal generation circuit.

[0044] Suppose a constitution that two nodes, the node A and the node B as shown in Fig.2, are connected by a serial port. The port C has a transmitting/a receiving block shown in Fig.1. During the usual operation, due to the noises and the like, an error of a boundary in the block code boundary detection circuit 12 within the receiving block 19 or loss of synchronization of the descrambler 15 (for example, the node A ① of Fig.2) is generated. In this case, since a main signal and a control signal outputted from the descrambler are different from signals which are expected, they are not processed by the network initiation/control state machine 21 of an upper layer. Specifically, the network initiation/control state machine 21 stops operation and becomes in a state of being locked(②). In the case where the locked state of the network initiation/control state machine 21 is continued more than a certain period of time (according to the IEEE 1394-1995, MAX_ARB_STATE_TIME=166.8us), the network initiation/control state machine 21 outputs a bus reset signal (0101) as a control signal for performing the initiation of the network(③).

[0045] In the node A, the bus reset detection circuit 6 which has detected a bus reset signal outputted from the network initiation/control state machine 21 outputs a signal for several clocks interval (for example, 6 clocks interval) for the purpose of switching an output of the selector B9 from an output of the 4B/10B conversion circuit 7 to an output of the bus reset identification code generation circuit.

[0046] The bus reset identification code generation circuit 8 generates and outputs a block code which is not used in a control signal and a main signal (for example, a code of 20 bits which alternately transmits two codes of K28.5+=0011111010 and K28.5-=1100000101). A bus reset identification code is serialized and outputted from the serial port without being randomized by the scrambler.

[0047] An appearance of a signal in each interface of the transmitting block is shown in Fig.3. In the case of a bus reset being generated, a bus reset signal (0101) is inputted as a control signal. Since a bus reset signal is randomized, a scrambler output and a 4B/10B conversion output do not have any regularities. When a control signal is changed into a bus reset signal, a bus reset detection circuit output is changed from "L" to "H", and after a certain period of time (for example, 6 clocks interval), changed from "H" to "L" again. A bus reset identification code is outputted from the selector C only for a certain period of time (for example, 6 clocks interval). A bus reset signal from the node A is inputted into the node B by way of the transmission path(④).

[0048] In the receiving block 19 of the node B, a received serial signal is converted into a parallel signal by the serial/parallel conversion circuit 10, the detection of the coincidence with a bus reset identification code is performed by the block code boundary detection circuit 12, and a boundary of a block code is recognized again. Moreover, by the bus reset identification code detection circuit 11, a bus reset identification code is detected, and concurrently with a setting a train bit of the descrambler, an output of the selector D17 is switched from an output of the descrambler 15 to an output of the bus reset signal generation circuit 16.

[0049] The descrambler 15 identifies an output of itself, in the case where a bus reset signal in series (0101) are detected, resets a train bit, and switches an output of the selector D from an output of the bus reset signal generation circuit 16 to an output of the descrambler 15.

[0050] An appearance of a signal in each interface of the receiving block is shown in Fig.4. When a bus reset identification code (for example, a code of 20 bits of K28.5+ or K28.5-) is detected in a serial/parallel conversion output, a bus reset signal (0101) is outputted as a control signal output by switching an output of the selector D to the side of the bus reset signal generation circuit concurrently with a train bit being changed from "L" to "H". When the value of a descrambler output is locked (for example, 3 clocks in series) by a bus reset signal (0101), an output of the selector D is switched

to the side of the descrambler as well as a train bit is changed from "H" to "L".

[0051] The network initiation/control state machine 21 of the node B detects a bus reset signal from the node A (⑤) and transmits a bus reset signal for the purpose of starting the initiation of the network (⑥). A serial bus reset signal to which a bus reset identification code is added is outputted from the transmitting block of the node B by the operation similar to that of the transmitting block of the node A and inputted into the node A by way of the transmission path (⑦).

[0052] The receiving block of the node A which receives a bus reset signal from the node B performs the re-detection of a block code boundary and the re-establishment of the synchronization between a scrambler and a descrambler and completes the initiation of the port during the bus resetting.

[0053] Next, the second embodiment of the present invention will be described below with reference to the drawings.

[0054] Fig.5 is a block diagram showing an encoding circuit of the second embodiment of the present invention.

[0055] In Fig.5, an encoding circuit is broadly divided into two (2) sections of the transmitting block 18 and the receiving block 19. The transmitting block 18 is composed of the selector A1, the scrambler 2, the 8B/10B conversion circuit 3, the 4B/10B conversion circuit 7, the selector C4 and the parallel/serial conversion circuit 5. The receiving block 19 is composed of the serial/paallel conversion circuit 10, the block code boundary detection circuit 12, the 10B/8B conversion circuit 14, the 10B/4B conversion circuit 13, the descrambler 15, the bus reset signal generation circuit 16 and the selector D17.

[0056] The selector A1 has a function of switching back and forth between a control signal and a main signal for the purpose of using the common scrambler by a control signal and a main signal.

[0057] The scrambler 2 has a function of randomizing a data sequence of control signals or main signals.

[0058] The 8B/10B conversion circuit 3 has a function of converting a main signal of 8 bits into a code of 10 bits.

[0059] The 4B/10B conversion circuit 7 has a function of converting a control signal of 4 bits into a code of 10 bits.

[0060] The bus reset detection circuit 6 has functions of detecting a bus reset signal in a control signal and outputting a trigger signal performing the re-detection of a block code boundary, and furthermore, outputting a signal for the purpose of switching the selector D9.

[0061] The selector C4 has a function of switching back and forth between a main signal and a control signal.

[0062] The parallel/serial conversion circuit 5 has a function of converting a parallel signal of 10 bits into a serial signal.

[0063] The serial/parallel conversion circuit 10 has a function of converting a serial signal from the transmission path into a parallel signal.

[0064] The block code boundary detection circuit 12 has functions of detecting a boundary of a block code (for example, a code of 10 bits) and outputting parallel signals in a block unit from a boundary to another boundary after the detection of a boundary, and furthermore, setting a train bit after the detection of a block code boundary.

[0065] The 10B/8B conversion circuit 14 has a function of converting a block code of 10 bits which is a main signal into a code of 8 bits.

[0066] The 10B/4B conversion circuit 13 has a function of converting a block code of 10 bits which is a control signal into a code of 4 bits.

[0067] The descrambler 15 has a function of converting a code randomized on the transmitting side into the original code which is not randomized.

[0068] The bus reset signal generation circuit 16 has a function of generating a bus reset signal (0101) as a control code.

[0069] The selector D has a function of switching back and forth between an output of the descrambler and an output of the bus reset signal generation circuit.

[0070] In the first embodiment of the present invention described above, a method that a first several clocks interval of a bus reset signal is replaced by a special code and transmitted so that the bus reset signal can be detected on the receiving side and the detection of a boundary of a block code and the re-establishment of the synchronization between a scrambler and a descrambler are performed by detecting this special code on the receiving side of the opposed node is employed. However, in the case where a bus reset signal was detected on the transmitting side, the problem of the prior art can be solved as well by the means that a trigger signal performing the re-detection of a block code boundary is outputted to the receiving side within the same node and a trigger signal performing the re-establishment of the synchronization between a scrambler and a descrambler is outputted after the re-detection of a block code boundary.

[0071] Suppose a case that two (2) nodes of the node A and the node B having an encoding circuit of Fig.5 are connected each other as in Fig.2. In the node A, the bus reset detection circuit 6 which has detected a bus reset signal from the network initiation/control state machine 21 outputs a trigger signal for the purpose of starting the re-detection of a block code boundary and outputs a signal for the purpose of switching an output of the selector D17 to an output of the bus reset signal generation circuit 16.

[0072] Moreover, a bus reset signal from the network initiation/control state machine 21 is randomized by the scrambler 2, and after this signal is block-encoded by the 4B/10B conversion circuit 7, this signal is converted into a serial signal and transmitted as a serial signal.

[0073] The node B which has received this serial signal detects a bus reset signal and the network initiation/control state machine of the node B outputs a bus reset signal as a control signal. This bus reset signal is transmitted to the node A and converted into a parallel signal by the serial/parallel conversion circuit.

[0074] In the block code boundary detection circuit 12 of the node A, the detection of a boundary is conventionally performed by detecting the coincidence with a control code C4 (=0010001111) or C11 (=1101110000).

[0075] The block code boundary detection circuit 12 sets a train bit for the purpose of performing the re-establishment of the synchronization between a scrambler and a descrambler after the completion of the detection of a boundary.

[0076] In the case where a stable (locked) bus reset code (for example, 3 clocks in series) from the descrambler 15 is obtained, a train bit is reset, an output of the selector D17 is switched to an output of the descrambler.

[0077] According to an encoding circuit of the present invention described above in detail, even in the case where an error of a boundary of a block code and loss of the synchronization between a scrambler and a descrambler are generated after the initiation of the port due to the noises and the like, the initiation of the port, specifically, the re-detection of a block code boundary and the re-establishment of the synchronization between a scrambler and a descrambler concurrently with the initiation of the network can be performed.

Claims

1. In an encoding circuit comprising a transmitting block(18) and a receiving block(19), said transmitting block having:

   a scrambler(2) randomizing a data sequence of a control signal from an upper layer and a data sequence of a main signal from an upper layer;
   a block encoding circuit(3, 7) block-encoding a control signal and a main signal respectively randomized by said scrambler ;
   a parallel/serial conversion circuit(5) converting a parallel signal outputted from said block encoding circuit into a serial signal;
   a bus reset identification code generation circuit(8) generating a bus reset identification code replacing a first several clocks interval of a bus reset signal performing an initiation of a network, said bus reset signal is included in a control signal from an upper layer; and
   a bus reset detection circuit(6) detecting said bus reset signal and making said bus reset identification code input into said parallel/serial conversion circuit;
   said receiving block having:
   a serial/parallel conversion circuit(10) converting a serial signal from a transmission path into a parallel signal;
   a block code boundary detection circuit(12) detecting a code boundary of a block code out of a parallel signal outputted from said serial/parallel conversion circuit and outputting a parallel signal in a block code unit;
   a block encoding inverse conversion circuit(13, 14) inversely converting a code of a control signal and a code of a main signal respectively which are block-encoded on a transmitting side;
   a descrambler(15) restoring a data sequence which is randomized;
   a bus reset identification code detection circuit(11) detecting said bus reset identification code and generating a trigger signal for starting a re-establishment of a synchronization between said scrambler and said descrambler;
   a bus reset signal generation circuit(16) generating a pseudo bus reset signal for being outputted to an upper layer while an establishment of a synchronization between said scrambler and said descrambler is performed; and
   a selector(17) switching back and forth between an output of said descrambler and an output of said bus reset signal generation circuit.

2. An encoding circuit as claimed in claim 1, wherein said bus reset identification code uses a code which is not used in said control signal and said main signal.

3. An encoding circuit as claimed in claim 1 or 2, wherein said transmitting block(18) has furthermore a selector(9) switching back and forth between an output of said block encoding circuit and said bus reset identification code.

4. In an encoding circuit comprising a transmitting block(18) and a receiving block(19), said transmitting block(18) having:

   a scrambler(2) randomizing a data sequence of a control signal from an upper layer and a data sequence of a main signal from an upper layer;
   a first selector(1) being made a data sequence of said control signal and a data sequence of said main signal

as inputs and outputting only any one of a data sequence of said control signal and a data sequence of said main signal;

a first converting means(3) for converting a main signal into a code of predetermined numeric bits;

a second converting means(7) for converting a control signal into a code of predetermined numeric bits;

a bus reset detection circuit(6) detecting a bus reset signal performing an initiation of a network, said bus reset signal is included in a control signal from an upper signal and outputting a bus reset detection signal;

a bus reset identification code generation circuit(8) generating a bus reset identification code for replacing a first several clocks interval of said bus reset signal with a code which is not used in said control signal and said main signal;

a second selector(9) being made an output of said second converting means and said bus reset identification code as inputs and outputting a bus reset identification code for said several clocks interval when said bus reset detection signal is inputted;

a third selector(4) switching back and forth between an output of said first converting means and an output of said second selector and outputting an output of said first converting means and an output of said second selector; and

a parallel/serial conversion circuit(5) converting a parallel signal outputted from said third selector into a serial signal;

said receiving block(19) having:

a serial/parallel conversion circuit(10) converting a serial signal from a transmission path into a parallel signal;

a bus reset identification code detection circuit(11) detecting said bus reset identification code out of an output of said serial/parallel conversion circuit and generating a trigger signal for starting a re-establishment of a synchronization between a scrambler and a descrambler;

a block code boundary detection circuit(12) detecting a code boundary of a block code out of a parallel signal from said serial/parallel conversion circuit and outputting a parallel signal in a block code unit;

a first inverse converting means(13) for inversely converting a code of a control signal outputted from said block code boundary detection circuit;

a second inverse converting means(14) for inversely converting a code of a main signal outputted from said block code boundary detection circuit;

a descrambler(15) performing a re-establishment of a synchronization using said trigger signal as well as restoring a randomized data sequence outputted from said first inverse converting means and said second inverse converting means;

a bus reset signal generation circuit(16) generating a pseudo bus reset signal for being outputted to an upper layer while a re-establishment of a synchronization between said scrambler and said descrambler is performed; and

a selector(17) switching an output of said descrambler and an output of said bus reset signal generation circuit by using a trigger signal of said bus reset identification code detection circuit.

5. In an encoding circuit comprising a transmitting block(18) and a receiving block(19), said transmitting block(18) having:

a scrambler(2) randomizing a data sequence of a control signal from an upper layer and a data sequence of a main signal from an upper layer;

a block encoding circuit(3,7) block-encoding a control signal and a main signal respectively which are randomized by said scrambler;

a parallel/serial conversion circuit(5) converting a parallel signal outputted from said block encoding circuit into a serial signal; and

a bus reset detection circuit(6) detecting a bus reset signal in a control signal and generating a trigger signal for starting a re-detection of a boundary of a block code;

said receiving block(19) having:

a serial/parallel conversion circuit(10) converting a serial signal from a transmission path into a parallel signal;

a block code boundary detection circuit(12) receiving a trigger signal from said bus reset detection circuit, starting a re-detection of a boundary of a block code and generating a trigger signal for starting a re-establishment of a synchronization between a scrambler and a descrambler;

a block code inverse conversion circuit(13, 14) inversely converting a code of a control signal and a code of a main signal which are block-encoded on a transmitting side;

a descrambler(15) receiving a trigger signal from said block code boundary detection circuit, starting a re-establishment of a synchronization between a scrambler and a descrambler and generating a switching signal for switching a control signal for being outputted to an upper layer when a bus reset signal was detected in an

output;
a bus reset signal generation circuit(16) generating a pseudo bus reset signal for being outputted to an upper layer; and
a selector(17) switching back and forth between an output of said descrambler and an output of said bus reset signal generating circuit.

6. In an encoding circuit comprising a transmitting block(18) and a receiving block(19), said transmitting block(18) having:

a scrambler(2) randomizing a data sequence of a control signal from an upper layer and a data sequence of a main signal from an upper layer;
a first selector(1) being made a data sequence of said control signal and a data sequence of said main signal as inputs and outputting only any one of a data sequence of said control signal or a data sequence of said main signal to said scrambler;
a first converting means(3) for converting a main signal into a code of predetermined numeric bits;
a second converting means(7) for converting a control signal into a code of predetermined numeric bits;
a bus reset detection circuit(6) detecting a bus reset signal in said control signal and generating a trigger signal for starting a re-detection of a boundary of a block code;
a second selector(4) switching back and forth between an output of said first converting means and an output of said second converting means and outputting an output of said first converting means and an output of said second converting means; and
a parallel/serial conversion circuit(5) converting a parallel signal outputted from said second selector into a serial signal;
said receiving block(19) having:
a serial/parallel conversion circuit(10) converting a serial signal from a transmission path into a parallel signal;
a block code boundary detection circuit(12) receiving a trigger signal from said bus reset detection circuit, starting a re-detection of a boundary of a block code and generating a trigger signal for starting a re-establishment of a synchronization between a scrambler and a descrambler after the detection of a boundary of a block code;
a first inverse converting means(13) for inversely converting a code of a control signal from said block code boundary detection circuit;
a second inverse converting means(14) for inversely converting a code of a main signal from said block code boundary detection circuit;
a descrambler(15) receiving a trigger signal from said block code boundary detection circuit, starting a re-establishment of a synchronization between a scrambler and a descrambler and generating a switching signal for switching a control signal for being outputted to an upper layer when a bus reset signal is detected in an output;
a bus reset generation circuit(16) generating a pseudo bus reset signal for being outputted to an upper layer; and
a selector(17) switching back and forth between an output from said descrambler and an output from said bus reset signal generation circuit.

7. A method of detecting a block code boundary and establishing a synchronization between a scrambler and a descrambler, said method comprising steps of:

detecting a bus reset signal performing an initiation of a network out of a control signal outputted from a network initiation/control state machine;
acknowledging a detection of said bus reset signal by using a signal which is not randomized to a receiving side; and
performing a re-detection of a block code boundary and a re-establishment of a synchronization between a scrambler and a descrambler when said acknowledgment is recognized on a receiving side.

8. A method of detecting a block code boundary and establishing a synchronization between a scrambler and a descrambler, said method comprising steps of:

detecting a bus reset signal performing an initiation of a network out of a control signal outputted from a network initiation/control state machine;
replacing a code of a first several clocks interval of said bus reset signal into a code which is not used in said control signal and said main signal and generating a bus reset identification code;

detecting said bus reset identification code and setting a train bit of a descrambler;

performing a re-detection of a block code boundary by using said bus reset identification code; and outputting a pseudo bus reset signal to a network initiation/control state machine while a re-establishment of a synchronization of said descrambler is performed.

9. A method of detecting a block code boundary and establishing a synchronization between a scrambler and a descrambler, said method comprising steps of:

detecting a bus reset signal performing an initiation of a network out of a control signal outputted from a network initiation/control state machine and generating a trigger signal for performing a re-detection of a block code boundary;

performing a re-detection of a block code boundary by using said trigger signal;

setting a train bit of a descrambler after a re-detection of a block code boundary; and

outputting a pseudo bus reset signal to a network initiation/control state machine during a re-detection of said block code boundary and a re-establishment of a synchronization of said descrambler.

FIG.1

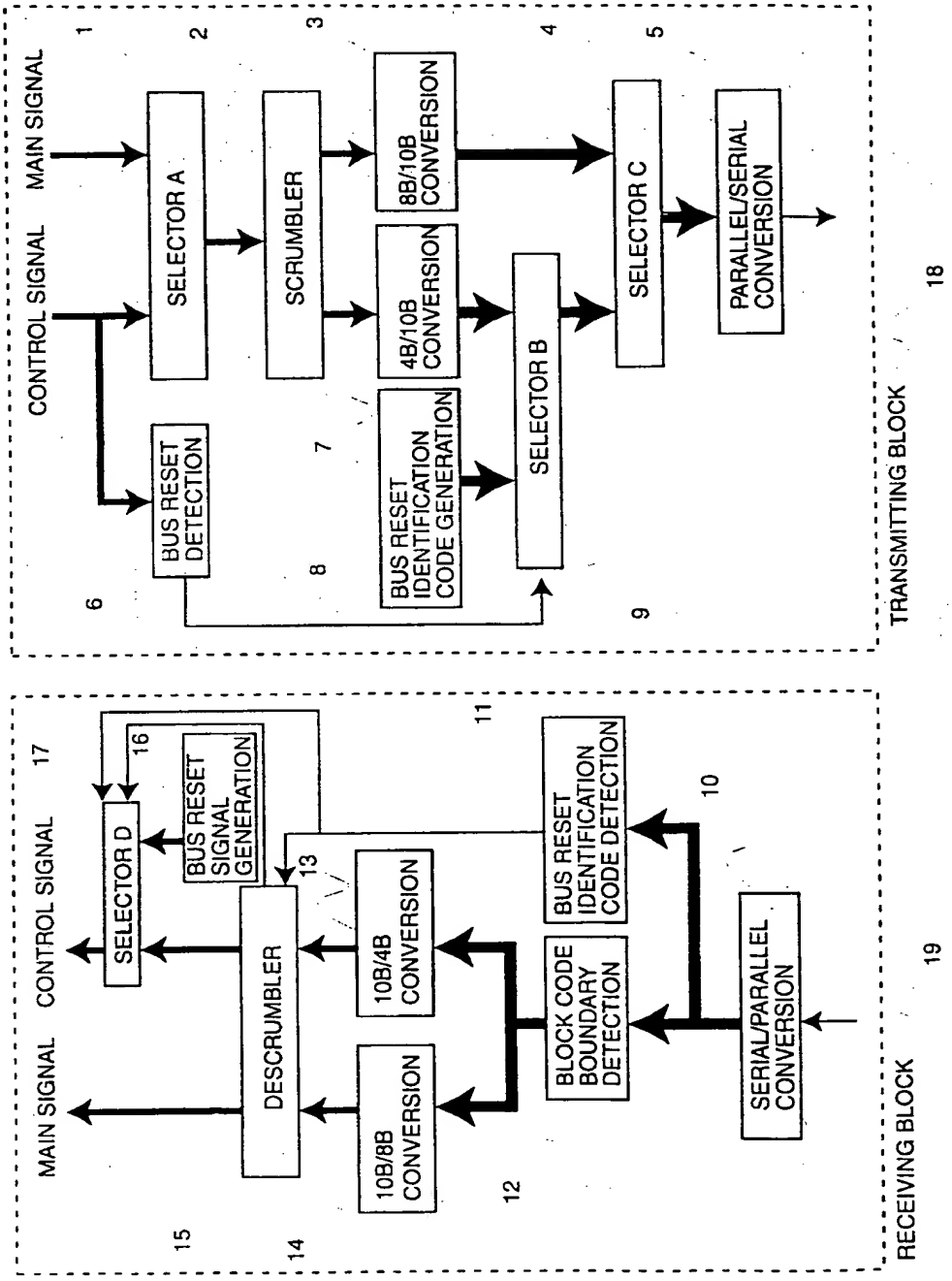
TRANSMITTING BLOCK
CONTROL SIGNAL
MAIN SIGNAL
SELECTOR A
SCRUMBLER
8B/10B CONVERSION
4B/10B CONVERSION
BUS RESET DETECTION
BUS RESET IDENTIFICATION CODE GENERATION
SELECTOR B
SELECTOR C
PARALLEL/SERIAL CONVERSION
1
2
3
4
5
6
7
8
9
RECEIVING BLOCK
MAIN SIGNAL
CONTROL SIGNAL
SELECTOR D
BUS RESET SIGNAL GENERATION
DESCRUMBLER
10B/4B CONVERSION
10B/8B CONVERSION
BLOCK CODE BOUNDARY DETECTION
BUS RESET IDENTIFICATION CODE DETECTION
SERIAL/PARALLEL CONVERSION
10
11
12
13
14
15
16
17
18
19

FIG.2

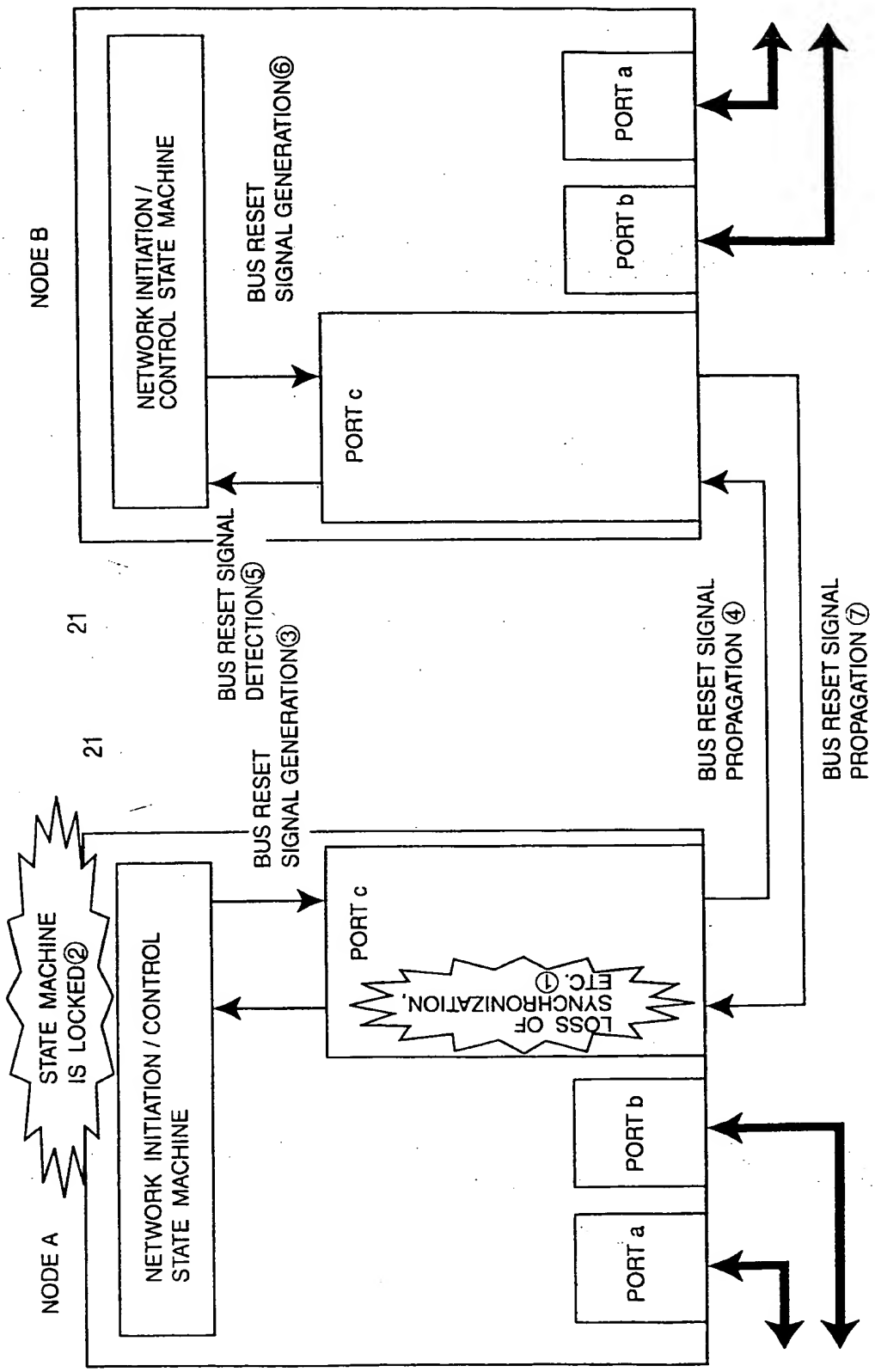
NODE A
NETWORK INITIATION / CONTROL STATE MACHINE
STATE MACHINE IS LOCKED②
PORT a
PORT b
PORT c
LOSS OF SYNCHRONIZATION, ETC.①
BUS RESET SIGNAL GENERATION③
21
BUS RESET SIGNAL DETECTION⑤
21
BUS RESET SIGNAL PROPAGATION ④
BUS RESET SIGNAL PROPAGATION ⑦
NODE B
NETWORK INITIATION / CONTROL STATE MACHINE
BUS RESET SIGNAL GENERATION⑥
PORT c
PORT b
PORT a

FIG.3

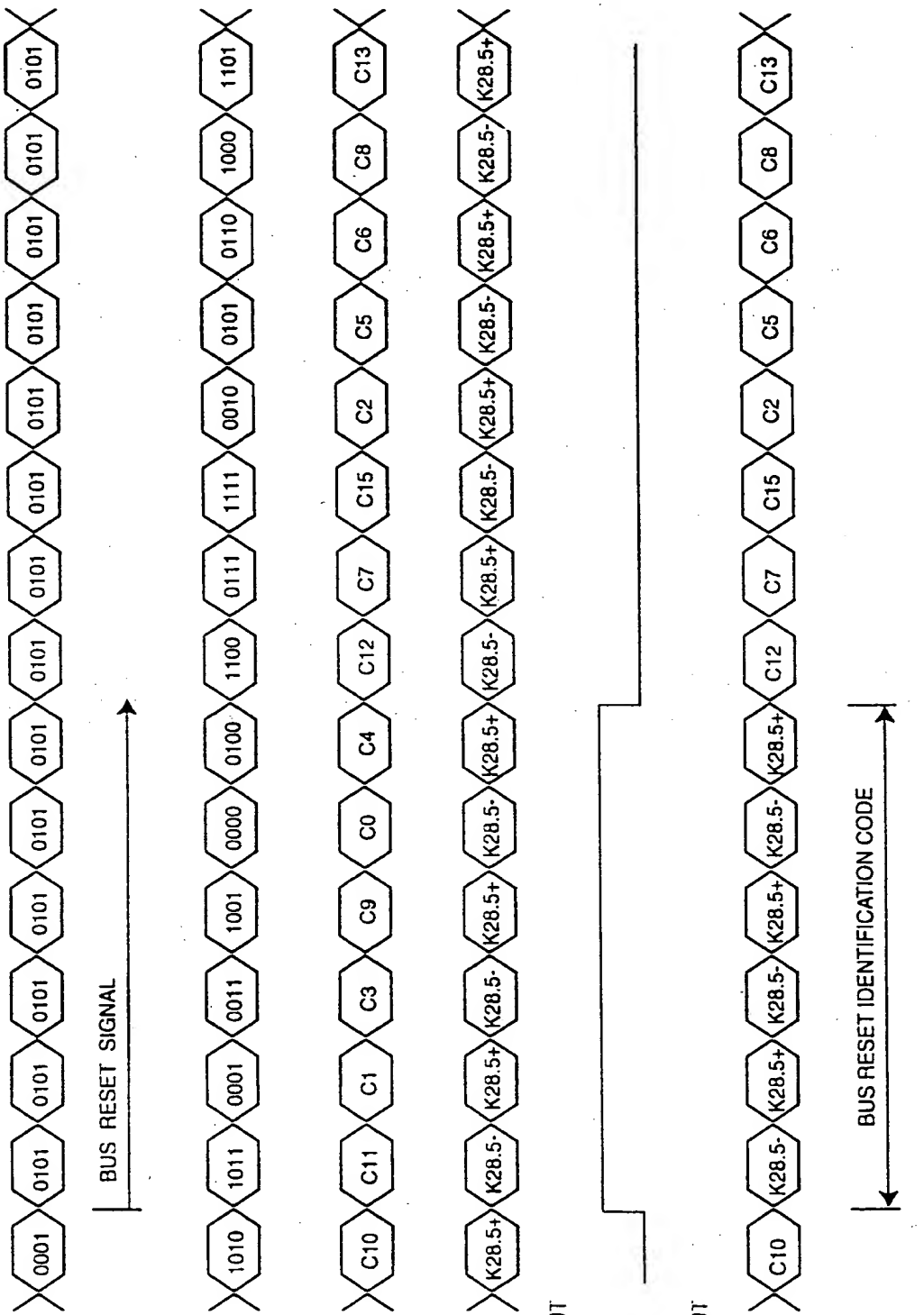
CONTROL SIGNAL
0001 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101
BUS RESET SIGNAL
SCRUMBLER OUTPUT
1010 1011 0001 0011 1001 0000 0100 1100 0111 1111 0010 0101 0110 1000 1101
4B / 10B CONVERSION OUTPUT
C10 C11 C1 C3 C9 C0 C4 C12 C7 C15 C2 C5 C6 C8 C13
BUS RESET IDENTIFICATION CODE GENERATION CIRCUIT OUTPUT
K28.5+ K28.5- K28.5+ K28.5- K28.5+ K28.5- K28.5+ K28.5- K28.5+ K28.5- K28.5+ K28.5- K28.5+ K28.5- K28.5+
BUS RESET IDENTIFICATION CODE DETECTION CIRCUIT OUTPUT
SELECTOR C OUTPUT
C10 K28.5- K28.5+ K28.5- K28.5+ K28.5- K28.5+ C12 C7 C15 C2 C5 C6 C8 C13
BUS RESET IDENTIFICATION CODE

FIG.4

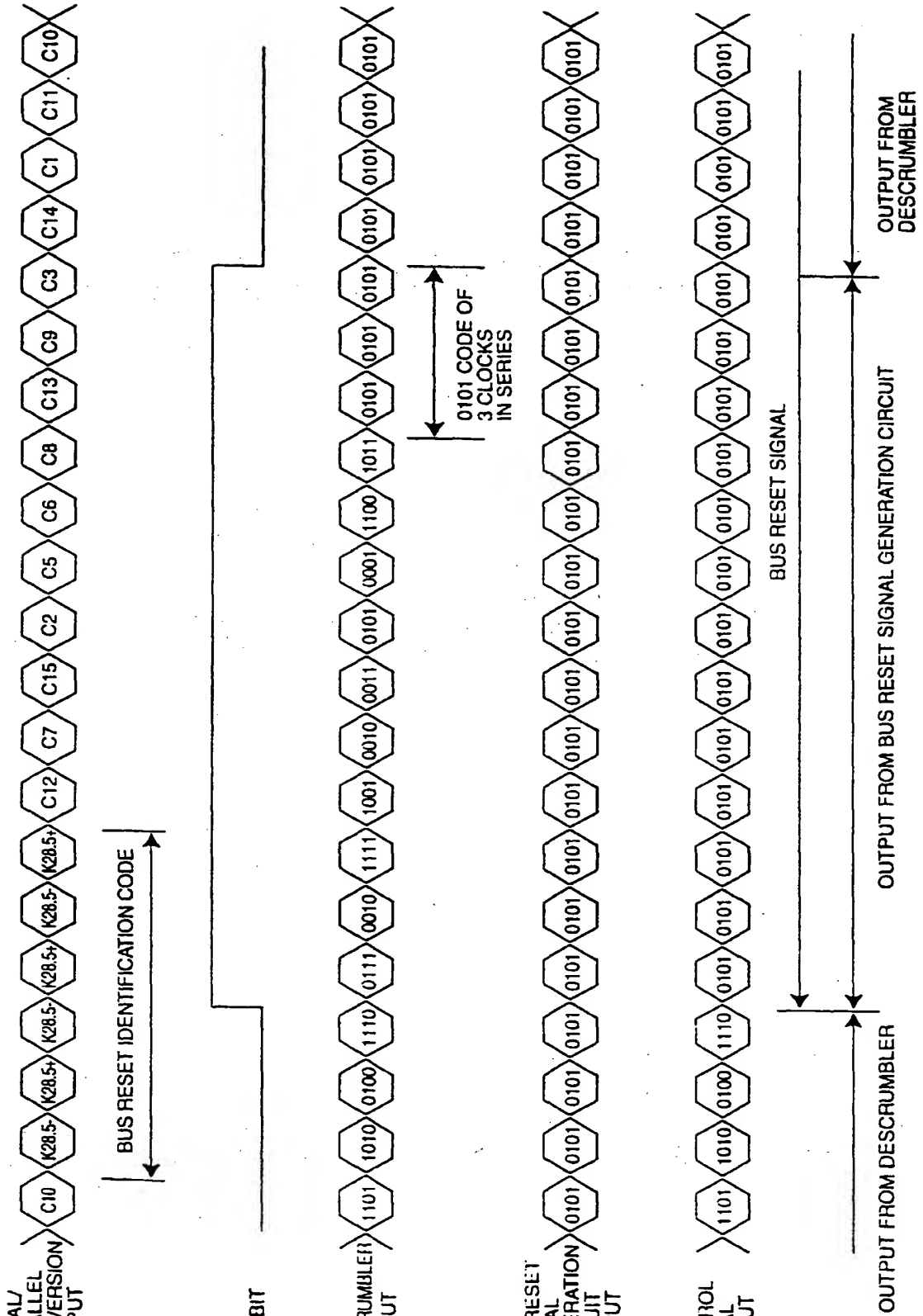
SERIAL/ PARALLEL CONVERSION OUTPUT
C10 K28.5- K28.5+ K28.5- K28.5+ K28.5- K28.5+ C12 C7 C15 C2 C5 C6 C8 C13 C9 C3 C14 C1 C11 C10
BUS RESET IDENTIFICATION CODE
Train BIT
DESCRUMBLER OUTPUT
1101 1010 0100 1110 0111 0010 1111 1001 0010 0011 0101 0001 1100 1011 0101 0101 0101 0101 0101 0101
0101 CODE OF 3 CLOCKS IN SERIES
BUS RESET SIGNAL GENERATION CIRCUIT OUTPUT
0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101
CONTROL SIGNAL OUTPUT
1101 1010 0100 1110 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101 0101
BUS RESET SIGNAL
OUTPUT FROM DESCRUMBLER
OUTPUT FROM BUS RESET SIGNAL GENERATION CIRCUIT
OUTPUT FROM DESCRUMBLER

FIG.5

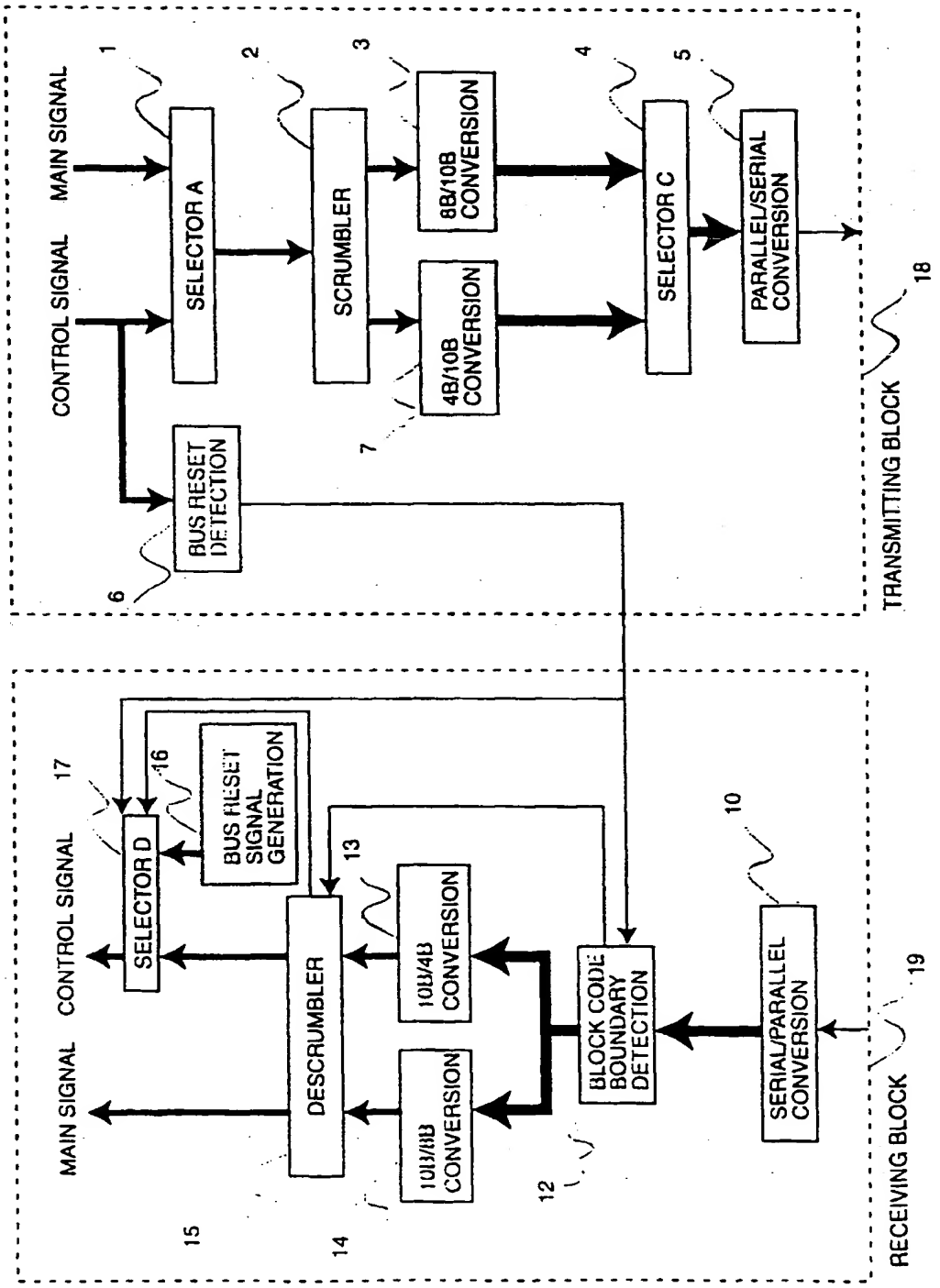
MAIN SIGNAL
CONTROL SIGNAL
SELECTOR A
SCRUMBLER
8B/10B CONVERSION
4B/10B CONVERSION
SELECTOR C
PARALLEL/SERIAL CONVERSION
BUS RESET DETECTION
TRANSMITTING BLOCK
MAIN SIGNAL
CONTROL SIGNAL
SELECTOR D
BUS RESET SIGNAL GENERATION
DESCRUMBLER
10B/8B CONVERSION
10B/4B CONVERSION
BLOCK CODE BOUNDARY DETECTION
SERIAL/PARALLEL CONVERSION
RECEIVING BLOCK
1
2
3
4
5
6
7
10
12
13
14
15
16
17
18
19

FIG.6

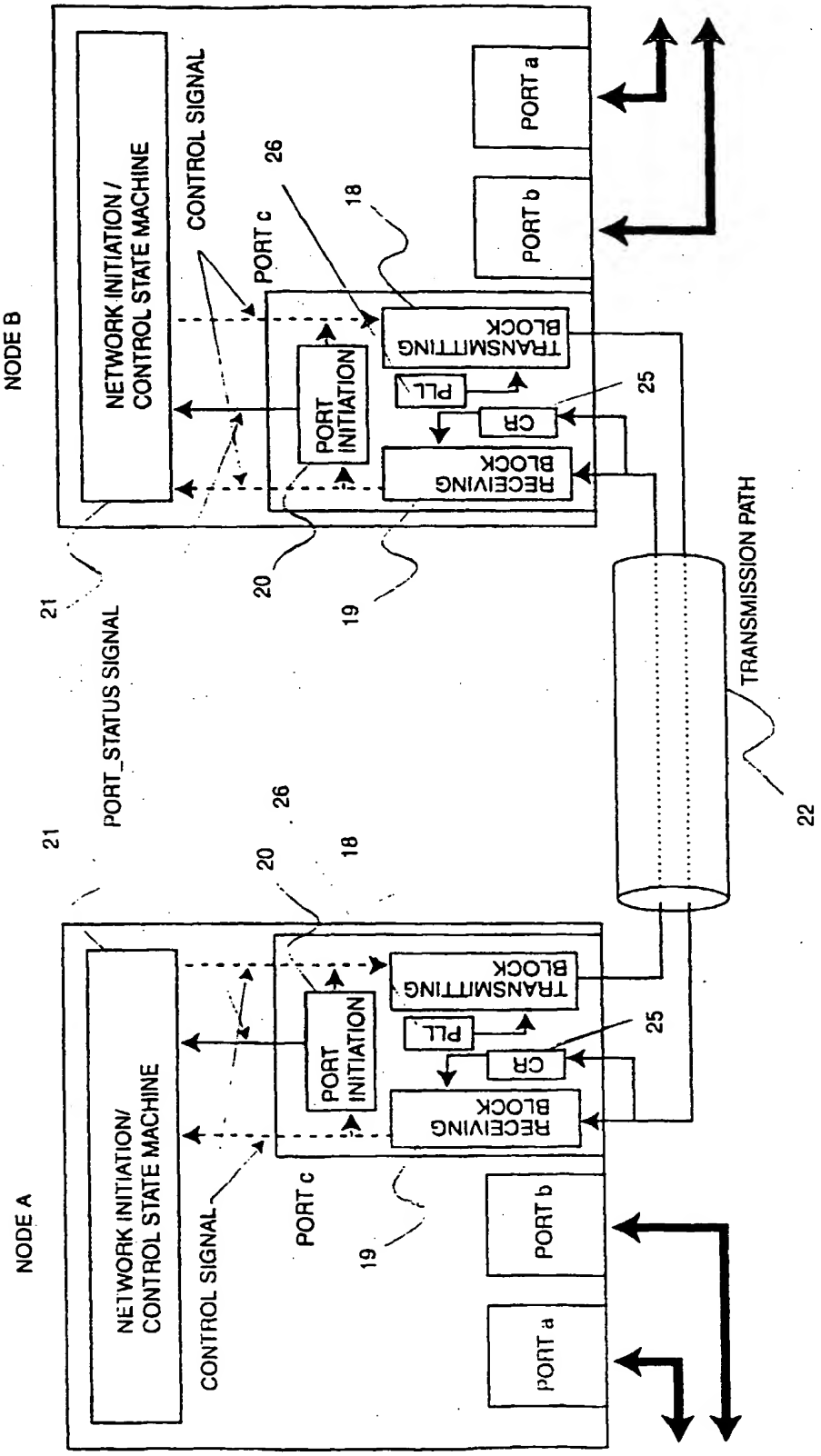
NODE B
NETWORK INITIATION / CONTROL STATE MACHINE
CONTROL SIGNAL
PORT c
26
18
PORT a
PORT b
PORT INITIATION
TRANSMITTING BLOCK
PLL
CR
RECEIVING BLOCK
25
21
20
19
PORT_STATUS SIGNAL
TRANSMISSION PATH
22
NODE A
NETWORK INITIATION/ CONTROL STATE MACHINE
CONTROL SIGNAL
PORT c
PORT b
PORT a

FIG.7

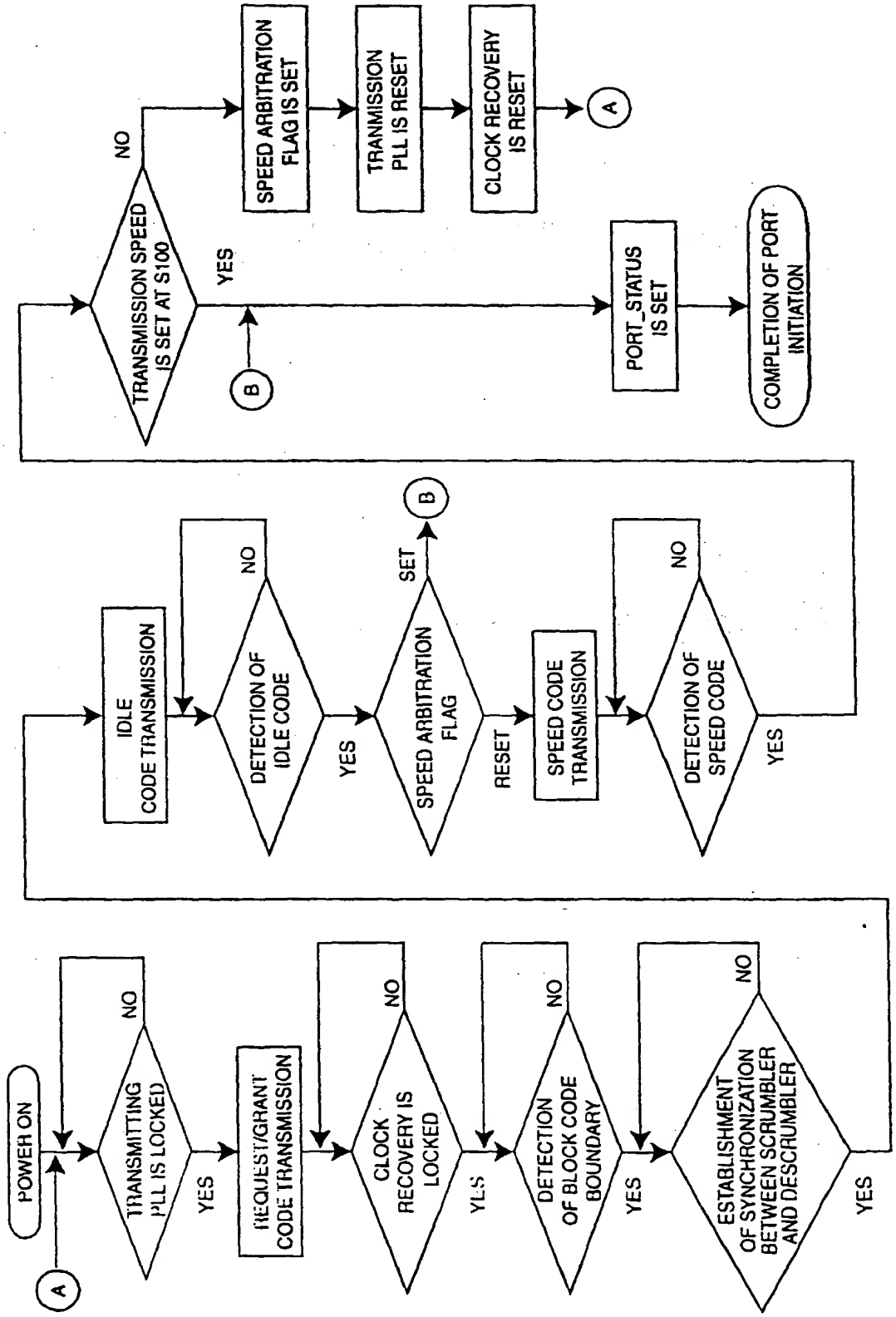
POWEH ON
A
TRANSMITTING PLL IS LOCKED
NO
YES
REQUEST/GRANT CODE TRANSMISSION
CLOCK RECOVERY IS LOCKED
NO
YES
DETECTION OF BLOCK CODE BOUNDARY
NO
YES
ESTABLISHMENT OF SYNCHRONIZATION BETWEEN SCRUMBLER AND DESCRUMBLER
NO
YES
IDLE CODE TRANSMISSION
DETECTION OF IDLE CODE
NO
YES
SPEED ARBITRATION FLAG
SET
B
RESET
SPEED CODE TRANSMISSION
DETECTION OF SPEED CODE
NO
YES
TRANSMISSION SPEED IS SET AT S100
NO
YES
B
SPEED ARBITRATION FLAG IS SET
TRANMISSION PLL IS RESET
CLOCK RECOVERY IS RESET
A
PORT_STATUS IS SET
COMPLETION OF PORT INITIATION

FIG.8

CONTROL SIGNAL CODE	SIGNIFICANCE OF CODE	CONTROL SIGNAL CODE	SIGNIFICANCE OF CODE
0 0 0 0	IDLE	1 0 0 0	SPEED-
0 0 0 1	REQUEST/GRANT	1 0 0 1	DATA_PREFIX+
0 0 1 0	PARENT_NOTIFY	1 0 1 0	DATA_END+
0 0 1 1	CHILD_NOTIFY	1 0 1 1	DATA_END-E
0 1 0 0	SPEED+	1 1 0 0	ESCAPE
0 1 0 1	RESET	1 1 0 1	reserved
0 1 1 0	DATA_END-	1 1 1 0	reserved
0 1 1 1	DATA_END+E	1 1 1 1	DATA_PREFIX-

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FIG.9

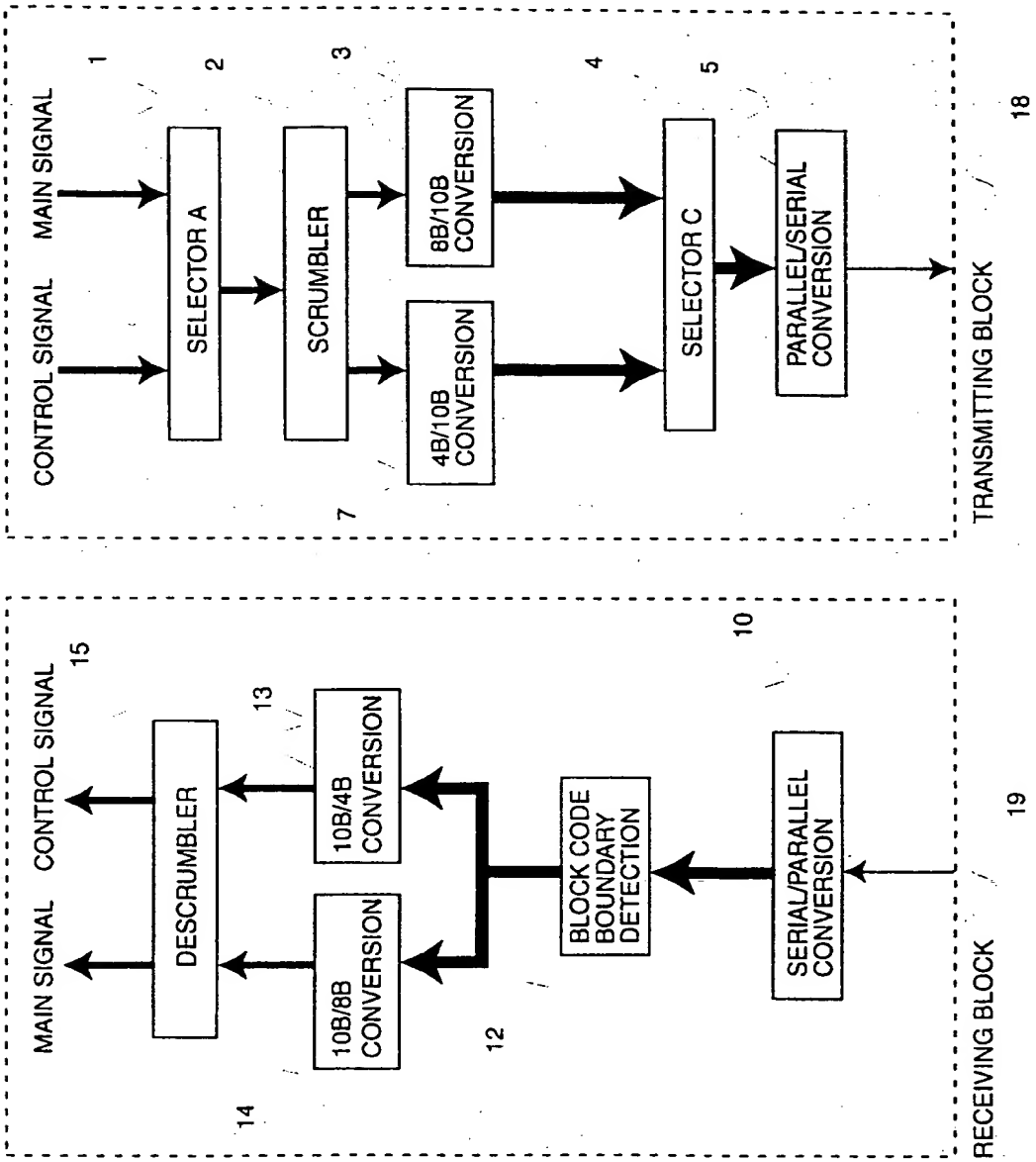
MAIN SIGNAL
CONTROL SIGNAL
1
SELECTOR A
2
SCRUMBLER
3
8B/10B CONVERSION
4B/10B CONVERSION
4
5
SELECTOR C
PARALLEL/SERIAL CONVERSION
7
TRANSMITTING BLOCK
18
10
SERIAL/PARALLEL CONVERSION
BLOCK CODE BOUNDARY DETECTION
12
10B/4B CONVERSION
10B/8B CONVERSION
13
DESCRUMBLER
15
MAIN SIGNAL
CONTROL SIGNAL
14
RECEIVING BLOCK
19

FIG.10

SCRUMBLER OUTPUT		4B/10B CONVERSION OUTPUT	SCRUMBLER OUTPUT		4B/10B CONVERSION OUTPUT
[S',R',Q',P']	SYMBOL		[S',R',Q',P']	SYMBOL	
0 0 0 0	C 0	0 0 0 0 0 1 1 1 1 1	1 0 0 0	C 8	0 1 1 1 1 1 0 0 0 0
0 0 0 1	C 1	0 0 0 0 1 0 1 1 1 1	1 0 0 1	C 9	1 0 1 1 1 1 0 0 0 0
0 0 1 0	C 2	0 0 0 0 1 1 1 1 1 0	1 0 1 0	C 1 0	0 0 1 1 1 1 1 0 0 0
0 0 1 1	C 3	0 0 0 1 0 0 1 1 1 1	1 0 1 1	C 1 1	1 1 0 1 1 1 0 0 0 0
0 1 0 0	C 4	0 0 1 0 0 0 1 1 1 1	1 1 0 0	C 1 2	1 1 1 0 1 1 0 0 0 0
0 1 0 1	C 5	1 1 0 0 0 0 0 1 1 1	1 1 0 1	C 1 3	1 1 1 1 0 0 0 0 0 1
0 1 1 0	C 6	0 1 0 0 0 0 1 1 1 1	1 1 1 0	C 1 4	1 1 1 1 0 1 0 0 0 0
0 1 1 1	C 7	1 0 0 0 0 0 1 1 1 1	1 1 1 1	C 1 5	1 1 1 1 1 0 0 0 0 0

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FIG. 11

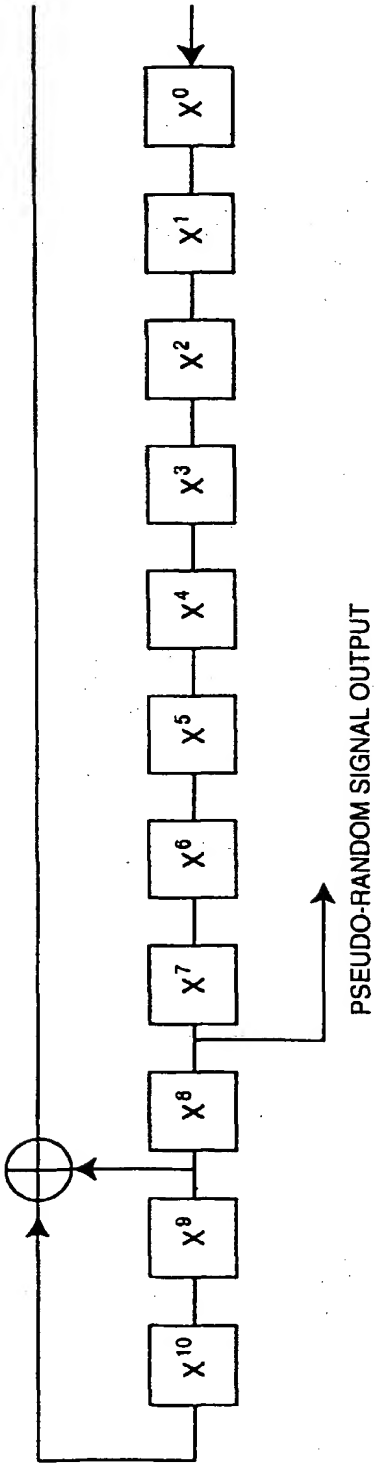

FIG.12

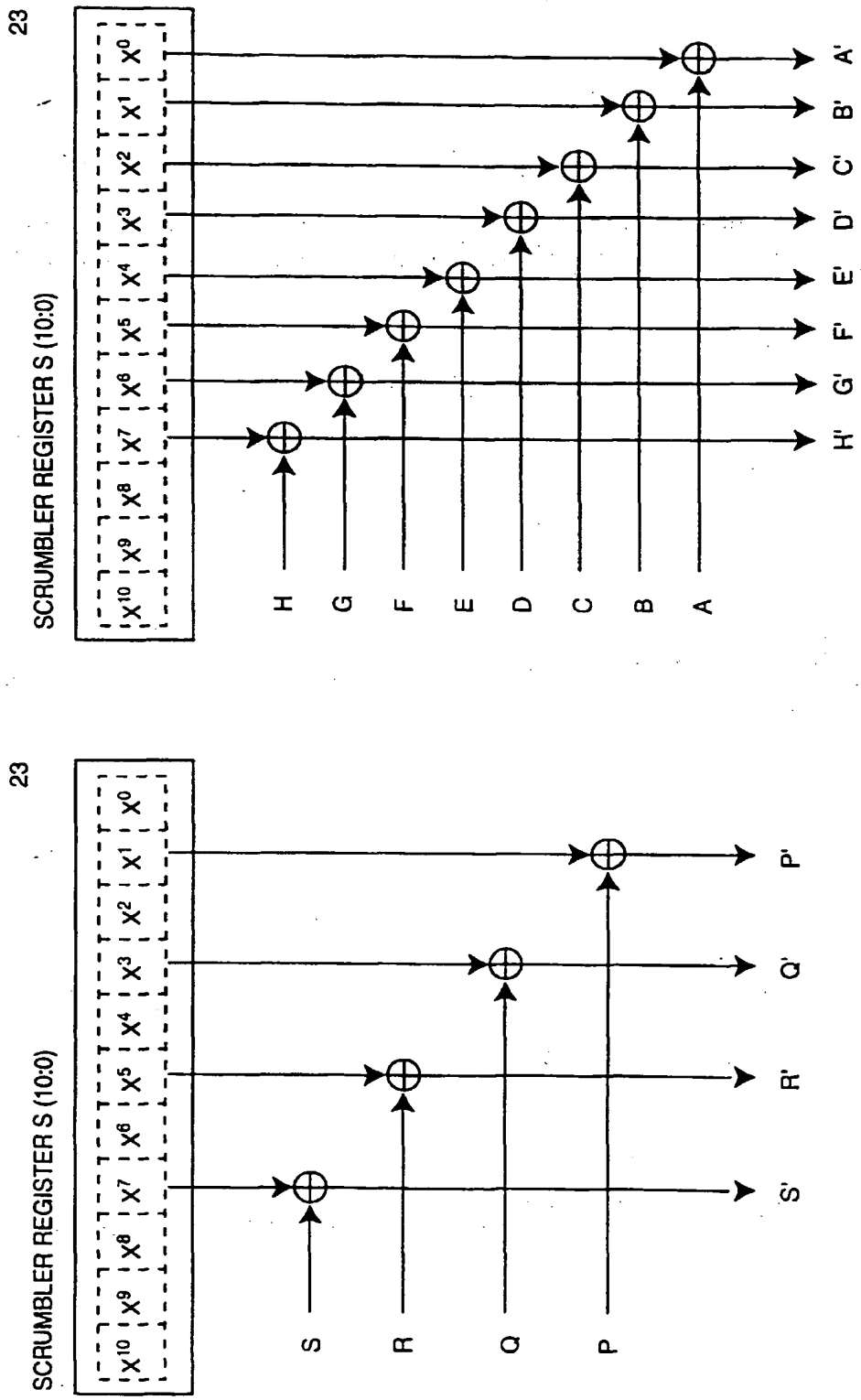
23
SCRUMBLER REGISTER S (10:0)
X10 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0
H G F E D C B A
H' G' F' E' D' C' B' A'
23
SCRUMBLER REGISTER S (10:0)
X10 X9 X8 X7 X6 X5 X4 X3 X2 X1 X0
S R Q P
S' R' Q' P'

FIG. 13

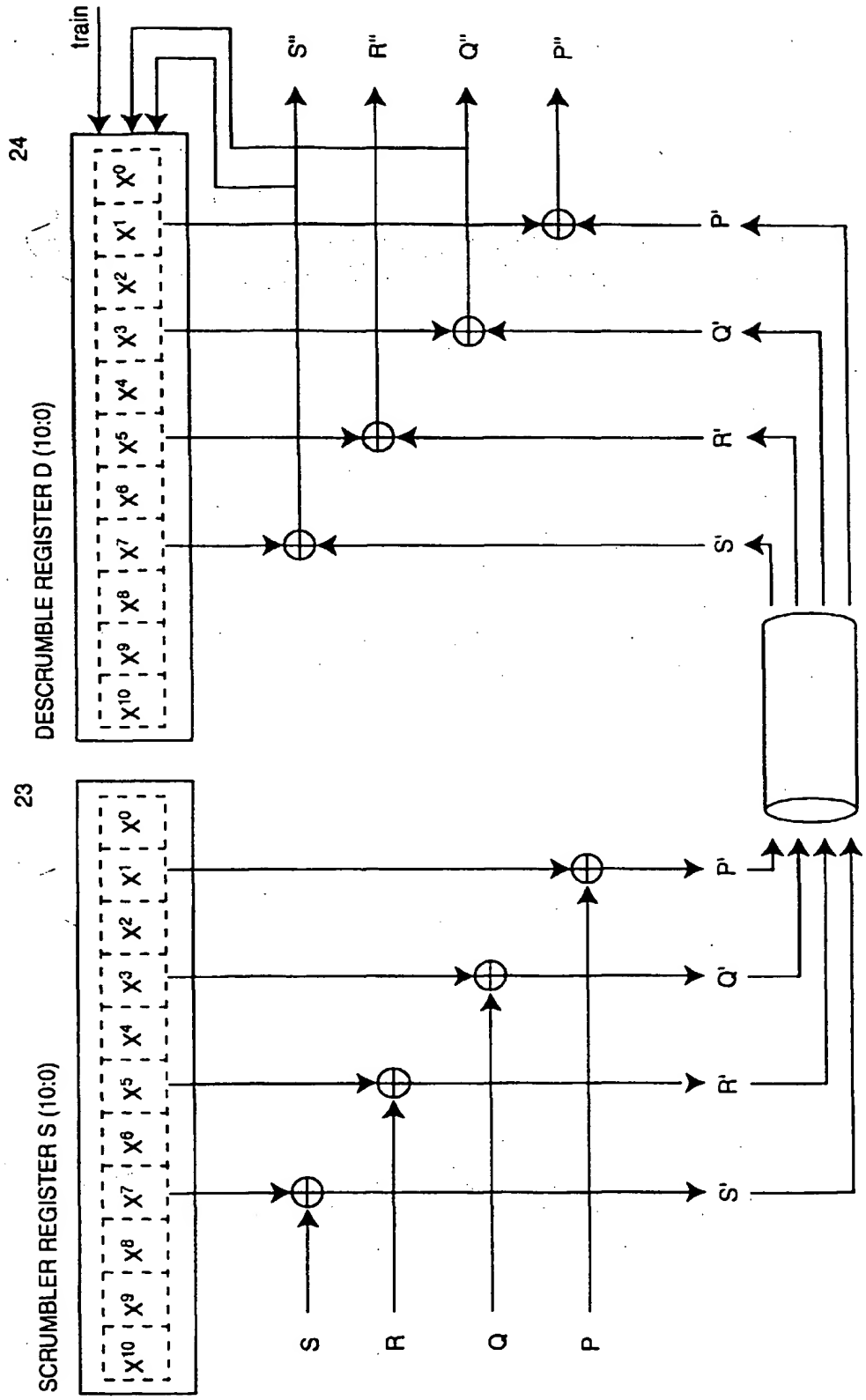
train
S''
R''
Q''
P''
24
DESCRUMBLE REGISTER D (10:0)
X0
X1
X2
X3
X4
X5
X6
X7
X8
X9
X10
P'
Q'
R'
S'
23
SCRUMBLER REGISTER S (10:0)
P'
Q'
R'
S'
S
R
Q
P

FIG 14

CLK	SCRUMBLER REGISTER S(10:0)	SCRUMBLER OUTPUT		DESCRUMBLER REGISTER D(10:0)	DESCRUMBLER OUTPUT
		[S',R',Q',P']	SYMBOL		[S",R",Q",P"]
0	10000000000	0001	c1	01001011111	0010
1	00010000000	1001	c9	11101100001	1101
2	00001010000	0001	c1	00100001100	0011
3	00000100010	0100	c4	10010100010	1001
4	01000010101	0001	c1	01010010101	1001
5	10101001000	0011	c3	10101001000	0001
6	00000001101	0011	c3	00000001101	0001
7	10100000111	0000	c0	10100000111	0001
8	11100100011	0100	c4	11100100011	0001
9	01101110101	0101	c5	01101110101	0001
10	10111010100	1001	c9	10111010100	0001
11	10001010000	0001	c1	10001010000	0001
12	00010100010	1100	c12	00010100010	0001

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